anticipated by Matsusaka et al. (US 4,959,510).

The Examiner rejected claims 2, 6, 7 and 27 under 35 U.S.C. §102(2) as being anticipated by Murakami et al. (US 6,031,292).

The Examiner rejected claim 5 under 35 U.S.C. §103(a) as being unpatentable over Matsusaka as applied to claims 2 and further in combination with Frey et al. (US 5,249,101).

The Examiner rejected claims 12, 13 and 34 under 35 U.S.C. §103(a) as being unpatentable over Matsusaka as applied to claims 3 and 11 and further in combination with Lee et al. (US 6,050,832) and Lan et al. (US 5,767,575).

The Examiner rejected claims 9 and 28 under 35 U.S.C. §103(a) as being unpatentable over Murakami as applied to claims 2 and 6 and further in combination with Sherman (US 5,784,262).

The Examiner rejected claims 10 and 29 under 35 U.S.C. §103(a) as being unpatentable over Murakami and Sherman as applied to claim 9 and further in combination with Tamaoki (JP 02-43748).

The Examiner rejected claims 30-35 under 35 U.S.C. §103(a) as being unpatentable over Murakami as applied to claim 6 and further in combination with Sambucetti (US 6,355,104).

Applicants respectfully traverse the §112, §102 and §103 rejections with the following arguments.

35 U.S.C. §112

The Examiner rejected claims 2-7, 9-13 and 27-35 under 35 U.S.C. §112, second paragraph, alleging that "[w]ith respect to claims 2 and 3, it is unclear how circuit lines can be

'totally external *aside* from being in contact with substrate.' The sentence with the word **aside**, in scope, includes an area of the line that is in the substrate and therefore not 'totally external' form the substrate."

Applicants disagree and respectfully contend that the phrase "aside from being in contact with the substrate" modifies the phrase "wherein the first circuit line is totally external to the substrate". Thus, Applicants respectfully contend that the feature of "wherein the first circuit line is totally external to the substrate aside from being in contact with the substrate" is unambiguously clear to one of ordinary skill in the art as well as to an ordinary person in general. Accordingly, Applicants respectfully maintain that the rejection of claims 2-7, 9-13 and 27-35 under 35 U.S.C. §112, second paragraph is improper.

35 U.S.C. §102

The Examiner rejected claims 2-4, 11, 33 and 35 under 35 U.S.C. §102(b) as being anticipated by Matsusaka et al. (US 4,959,510), alleging that "Matsusaka (Fig 1-3) discloses an electronic structure comprising: a substrate (11), a first circuit line (a portion of 4 that defines a line) including an inherent first conductive pad (region of line in contact with bump) and having a first thickness extending in a direction perpendicular to a surface of the substrate at which the first circuit line is coupled to the substrate, and wherein the first circuit line is inherently totally external to the substrate aside from being in contact with the substrate ('on substrate'; Column 2, Lines 47-49) and a second circuit line (2b) including an inherent second conductive pad and having a second thickness extending in a direction perpendicular to a surface of the substrate at which the second circuit line is coupled to the substrate, wherein the second circuit line is

electrically coupled the first signal line (via chip) and a thickness of the second circuit line is unequal to the first thickness, wherein the second circuit line is inherently totally external to the substrate aside from being in contact with the substrate ('on substrate'; Column 2, Lines 47-49), and the first line is in direct mechanical contact with the second circuit line (Column 2, Lines 39-42); wherein an end of the first circuit line includes a conductive pad and the end of the second circuit line includes a conductive pad; wherein the first conductive pad includes a metallic layer (12), and further comprising a first metallic coating (13) over the metallic layer and a second metallic coating over the first (14) wherein the first metallic coating inhibits diffusion of a metal from the second metallic coating into the metallic layer; a third circuit line (3) having a thickness that is unequal to the first and second thickness, and wherein the third line is inherently electrically coupled and in direct mechanical contact to the first line (third line forms a part of first line) and is electrically and in direct mechanical contact to the second circuit line (via soldering of chip, 5a)."

Applicants respectfully contend that Matsusaka does not anticipate claim 2, because Matsusaka does not teach each and every feature of claim 2. For example, Matsusaka does not teach "wherein the first circuit line is in **direct** mechanical contact with the second circuit line" (emphasis added). The Examiner alleges that Matsusaka teaches a first circuit line 4 and a second circuit line 2b. The Examiner has cited col. 2, lines 39-42 of Matsusaka which states that "[t]he solder bumps 52 of the first set are soldered to bonding pads 4 on the signal line conductors 3. The solder bumps 51 of the second set are soldered to a second power supply conductor 2b." Applicants contend, however, that the preceding citation in combination with Figure 2 of

Matsusaka merely demonstrates that the circuit lines 4 and 2b are coupled with each other through the chip 5a, and that Matsusaka does not teach that the circuit lines 4 and 2b are in **direct** mechanical contact with each other. Based on the preceding argument, Applicants respectfully maintain that Matsusaka does not anticipate claim 2 and that claim 2 is in condition for allowance. Since claims 4 and 11 depend from claim 2, Applicants contend that claims 4 and 11 are likewise in condition for allowance.

Applicants respectfully contend that Matsusaka does not anticipate claim 3, because Matsusaka does not teach each and every feature of claim 3. For example, Matsusaka does not teach "wherein the third circuit line has a third thickness that is unequal to ... the first thickness [of the first circuit line]... ". The Examiner alleges that Matsusaka teaches a first circuit line 4, a second circuit line 2b, and a third circuit line 3. Applicants contend, however, that in FIG. 2 the third circuit line 3 and the first circuit line 4 appear to have identical geometry with respect to thickness, and therefore do not satisfy the thickness limitations in claim 3. The Examiner has not made even a single argument to support the Examiner's allegation that the third circuit line 3 has a thickness that is unequal to the thickness of the first circuit line. Based on the preceding argument, Applicants respectfully maintain that Matsusaka does not anticipate claim 3 and that claim 3 is in condition for allowance. Since claims 33 and 35 depend from claim 3, Applicants contend that claims 33 and 35 are likewise in condition for allowance.

The Examiner rejected claims 2, 6, 7 and 27 under 35 U.S.C. §102(2) as being anticipated by Murakami et al. (US 6,031,292), alleging that "Murakami (Fig 1-3) discloses an electronic

structure comprising: a substrate (1), a first circuit line including an inherent conductive pad (3) and having a first thickness extending in a direction perpendicular to a surface of the substrate at which the first circuit line is coupled to the substrate, and wherein the first circuit line is totally external to the substrate aside from being in contact with the substrate, and a second circuit line (6) including a second inherent conductive pad and having a second thickness extending in a direction perpendicular to a surface of the substrate at which the second circuit line is coupled to the substrate, wherein the second circuit line is electrically coupled the first signal line via the first circuit line is coupled a first end of a plated through hole (5) and a second circuit line is coupled to a second end of the PTH, wherein a thickness of the second circuit line is unequal to the first thickness, wherein the second circuit line is totally external to the substrate aside from being in contact with the substrate, and the first line is inherently in direct mechanical contact with the second circuit line (via Plated Through Hole); wherein the first circuit line is coupled to a top surface of the substrate and the second circuit line is coupled to a bottom surface of the substrate."

Applicants respectfully contend that Murakami does not anticipate claim 2, because Murakami does not teach each and every feature of claim 2. For example, Murakami does not teach "wherein the first circuit line is in **direct** mechanical contact with the second circuit line" (emphasis added). The Examiner alleges that Murakami teaches a first circuit line 3 and a second circuit line 6. In conjunction with Figure 3 of Murakami, the Examiner has alleged that the first circuit line 3 is inherently in direct mechanical contact with the second circuit line 6 via the plated through hole 4. Applicants contend, however, that the circuit lines 6 and 3 are merely coupled with each other through the plated through hole 4, and that Murakama does not teach that the

circuit lines 6 and 3 are in **direct** mechanical contact with each other. Based on the preceding argument, Applicants respectfully maintain that Murakami does not anticipate claim 2 and that claim 2 is in condition for allowance. Since claims 6, 7 and 27 depend from claim 2, Applicants contend that claims 6, 7 and 27 are likewise in condition for allowance.

35 U.S.C. §103

The Examiner rejected claim 5 under 35 U.S.C. §103(a) as being unpatentable over Matsusaka as applied to claims 2 and further in combination with Frey et al. (US 5,249,101). Since claim 5 depends from claim 2, which Applicants have *supra* argued to be patentable under 35 U.S.C. §102, Applicants maintain that claim 5 is not unpatentable under 35 U.S.C. §103(a).

The Examiner rejected claims 12, 13 and 34 under 35 U.S.C. §103(a) as being unpatentable over Matsusaka as applied to claims 3 and 11 and further in combination with Lee et al. (US 6,050,832) and Lan et al. (US 5,767,575). Since claims 12 and 13 depend from claim 2, which Applicants have *supra* argued to be patentable under 35 U.S.C. §102, Applicants maintain that claims 12 and 13 are not unpatentable under 35 U.S.C. §103(a). Since claim 34 depends from claim 3, which Applicants have *supra* argued to be patentable under 35 U.S.C. §102, Applicants maintain that claim 34 is not unpatentable under 35 U.S.C. §103(a).

The Examiner rejected claims 9 and 28 under 35 U.S.C. §103(a) as being unpatentable over Murakami as applied to claims 2 and 6 and further in combination with Sherman (US

5,784,262). Since claims 9 and 28 depend from claim 2, which Applicants have *supra* argued to be patentable under 35 U.S.C. §102, Applicants maintain that claims 9 and 28 are not unpatentable under 35 U.S.C. §103(a).

The Examiner rejected claims 10 and 29 under 35 U.S.C. §103(a) as being unpatentable over Maurakami and Sherman as applied to claim 9 and further in combination with Tamaoki (JP 02-43748). Since claims 10 and 29 depend from claim 2, which Applicants have *supra* argued to be patentable under 35 U.S.C. §102, Applicants maintain that claims 10 and 29 are not unpatentable under 35 U.S.C. §103(a).

The Examiner rejected claims 30-35 under 35 U.S.C. §103(a) as being unpatentable over Murakami as applied to claim 6 and further in combination with Sambucetti (US 6,355,104). Since claims 30-32 depend from claim 2, which Applicants have *supra* argued to be patentable under 35 U.S.C. §102, Applicants maintain that claims 30-32 are not unpatentable under 35 U.S.C. §103(a). Since claims 33-35 depend from claim 3, which Applicants have *supra* argued to be patentable under 35 U.S.C. §102, Applicants maintain that claims 33-35 are not unpatentable under 35 U.S.C. §103(a).

Additionally, Applicant contends that Sambucetti cannot be used as prior art in rejecting claims of the present patent application, because the present patent application is a divisional application of parent application 09/344,031 filed 06/25/1999. Thus the present patent application has an effective filing date of 06/25/1999 which precedes the filing date of 02/22/2000 of the Sambucetti patent. Accordingly, Applicant respectfully maintains that Sambucetti cannot be used

as a prior art reference, and the rejection of claims 30-35 under 35 U.S.C. §103(a) is improper.

Additionally, Applicant contends that Sambucetti cannot be used as prior art in rejecting claims of the present patent application, because "[e]ffective November 29, 1999, subject matter which was prior art under former 35 U.S.C. 103 via 35 U.S.C. 102(e) is now disqualified as prior art against the claimed invention if that subject matter and the claimed invention 'were, at the time the invention was made, owned by the same person or subject to assignment by the same person.'" MPEP 706.02(1)(1). First, the present patent was filed on March 16, 2000 which is after November 29, 1999. Second, the Sambucetti patent is being considered by the Examiner as prior art under former 35 U.S.C. 103 via 35 U.S.C. 102(e), because the Sambucetti patent issued on January 1, 2002 which is after the filing date of March 16, 2000 of the present patent application. Third, both the subject matter of Sambucetti patent and the claimed invention of the present patent application were, at the time the invention was made, owned by International Business Machines Corporation or subject to assignment by International Business Machines Corporation. Accordingly, Applicant respectfully maintains that Sambucetti cannot be used as a prior art reference, and the rejection of claims 30-35 under 35 U.S.C. §103(a) is improper.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all claims 2-7, 9-13 and 27-35 meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact Applicants' representative at the telephone number listed below.

Date: 11/15/2002

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Appendix A. Identification of Amended Material

Please amend claims 29, 31, 32, and 34 as follows:

29. (ONCE AMENDED) The electronic structure of claim [15] 28, wherein a diameter of the second solder ball is unequal to a diameter of the first solder ball.

31. (ONCE AMENDED) The electronic structure of claim [17] 30, further comprising:

a wirebond interconnect coupled to the first conductive pad at the second metallic coating;

an electronic assembly coupled to the wirebond interconnect;

a solder ball coupled to the second conductive pad; and

an electronic carrier coupled to the solder ball.

32. (ONCE AMENDED) The electronic structure of claim [18] 31, wherein the metallic layer includes copper, wherein the first metallic coating includes nickel, wherein the metal of the second metallic coating is selected from the group consisting of gold and palladium, and wherein the wirebond interconnect includes a gold wire.

34. (ONCE AMENDED) The electronic structure of claim [20] 33, further comprising:

a wirebond interconnect coupled to the first conductive pad at the second metallic coating;

an electronic assembly coupled to the wirebond interconnect;

a solder ball coupled to the second conductive pad; and

an electronic carrier coupled to the solder ball.